# Non-Volatile Memory Using High k Dielectric

## EEPROM/Flash Memories Using $Al_2O_3$ Layer

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***Abstract*— Electrically Erasable Programmable Read Only Memory (EEPROM) are memory devices that store data byte by byte. In these devices a control gate and a floating gate is used for the device program/erase operation. Silicon Dioxide ($SiO_2$) layer is used as dielectric in these devices. As Aluminum Oxide ($Al_2O_3$) has higher dielectric constant than Silicon Dioxide ($SiO_2$) using it might be benificial in terms of device speed, compatibility and performance. The partial florination of $Al_2O_3$ gate dielectrics was observed when oxide-nitride-aluminum oxide (ONA) stack was exposed to a low energy florine beam. The electrical properties such as leakage current and memory window characteristics were improved possibly due to improved charge trapping characteristics through the formation of an $AlO_xF_y$ layer on the $Al_2O_3$ without changing the blocking layer thickness [2][4].**

### BACKGROUND & INTRODUCTION

The early work on floating gate EEPROM was demonstrated in late 1970's and an electrically erasable device using a thin gate oxide and Fowler-Nordheim tunneling for writing and erasing was proven. Eli Harari, one of the pioneer's in EEPROM/Flash memory devices studied the charge trapping effects in thin films of $Al_2O_3$ & $SiO_2$ in 1973. In his subsequent years he published papers which showed that thin $SiO_2$ films of about 100 Å were an efficient and reliable electron conduction mechanism for program and erase operations. Eli's 1977 JAP paper showed that the 1976 EEPROM was reliable, manufacturable, highly efficient and had high durability [3].

Electrically Erasable Programmable Read Only Memory (EEPROM) is a special type of memory device that can be erased by exposing it to an electrical charge. As it is a non-volatile type of memory, it stores the data even when the charge on the device is taken off. The EEPROM memory devices use Silicon Dioxide ($SiO_2$) as the dielectric layer by growing it over the substrate. Over the years as the transistors have scaled down in size, the thickness of silicon dioxide layer has remarkably reduced to hamper the device parameters by raising device performance. As it is arduous to mantain stability of thin oxide films, below a certain thickness of 2nm, leakage current due to tunneling increase considerably, leading to high power consumption and reduced device reliability. This replacing the oxide layer with high k dielectric material allows increased gate capacitance without the leakage effect [1].

### LITERATURE REVIEW

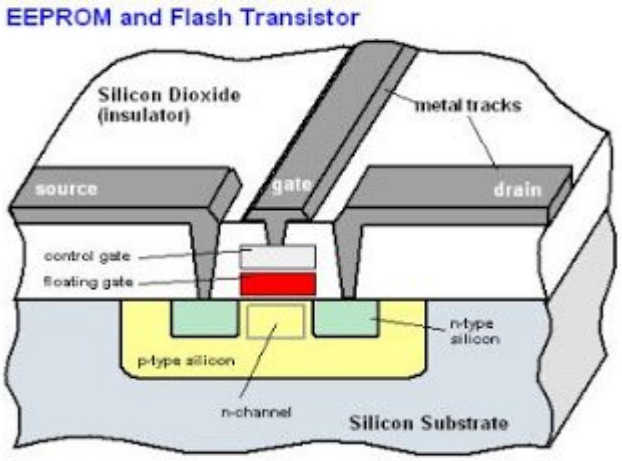


Fig 1

As shown in fig 1 the floating gate is a crutial part of the device. A floating gate can be fabricated by electrically isolating the gate so that there is no resistive connection to its control gate. A thin $SiO_2$ layer is to be maintained between the channel and floating gate. A number of secondary gates or inputs are then deposited above the floating gate and are electrically isolated from it. These inputs are only capacitively connected to floating gate, since it is completely surrounded by high resistive material. So in terms of its DC operating point floating gate is a floating node.

EEPROM uses the same principle as UV-EPROM. Electrons trapped in a floating gate will modify the characteristics of a cell, and so a logic 0 or a logic 1 will be stored. The more commom cell is composed of 2 transistors. The storage transistor has a floating gate that will trap electrons. In addition there is an access transistor which is required for operations. EEPROM's are erased when the electrons are trapped in floating gate.

In the non-volatile memory devices, the principle of MNOS (Metal-silicon Nitride-silicon Dioxide-silicon) is used where charges are stored in deep energy states at or near the interface between 2 gate dielectrics. Tunneling of electrons from the thin $SiO_2$ layer to the floating gate and back helps the device work. Due to small amount of trapping sites, only few of the charges will be captured at the interface centres. To capture more of these charges, there must be an increased current density which requires a greater write erase voltage or a thinner $SiO_2$ layer .

However, if the voltage on control gate is large, there is a degradation in the usefulness or wearout of the device. Similarly, as mentioned earlier growing a thin film oxide without defects is a tedious task [5]. Thus the propostion of using a high k material could prove to be an improvement in the device characteristics.

**PROPOSED METHOD**

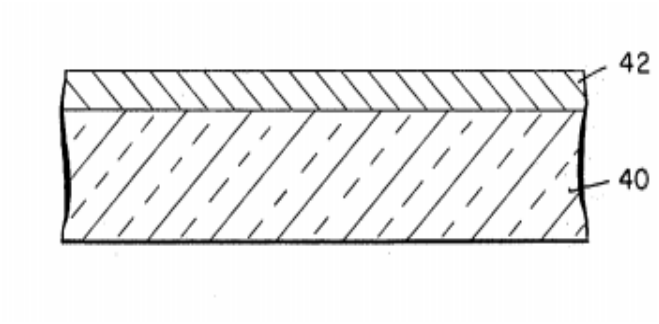


Fig 2.1

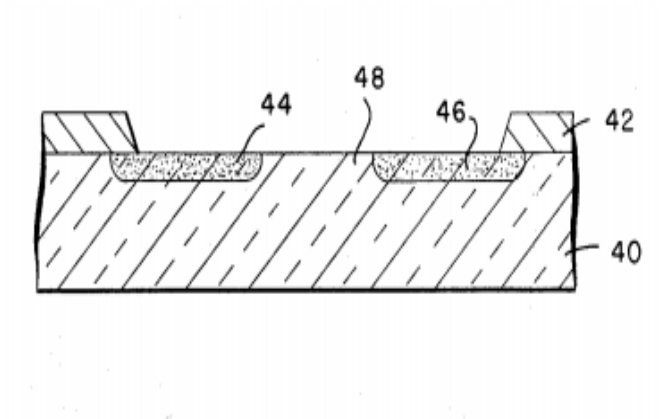


Fig 2.2

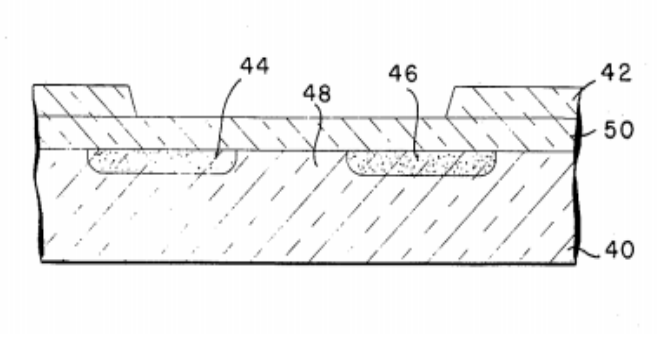


Fig 2.3

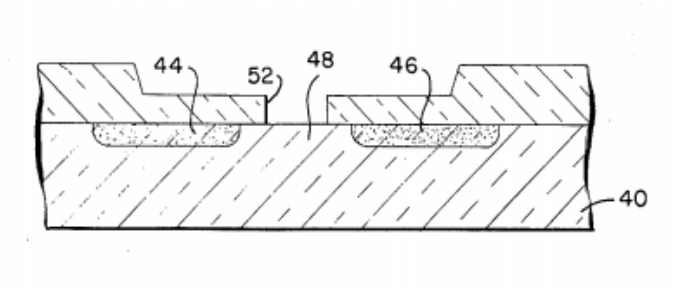


Fig 2.4

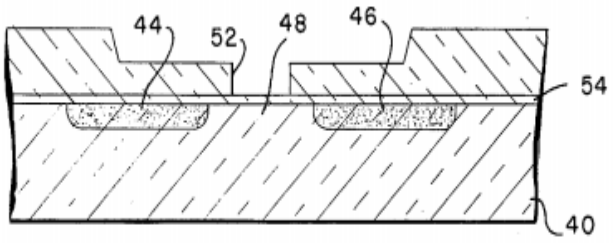


Fig 2.5

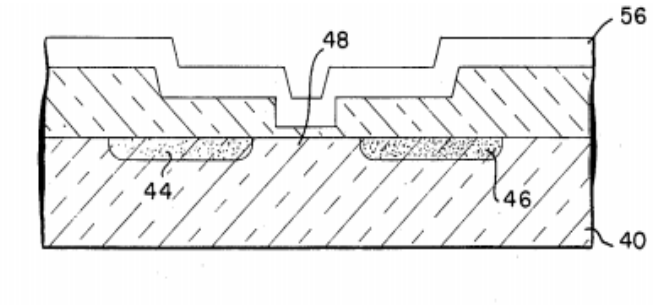


Fig 2.6

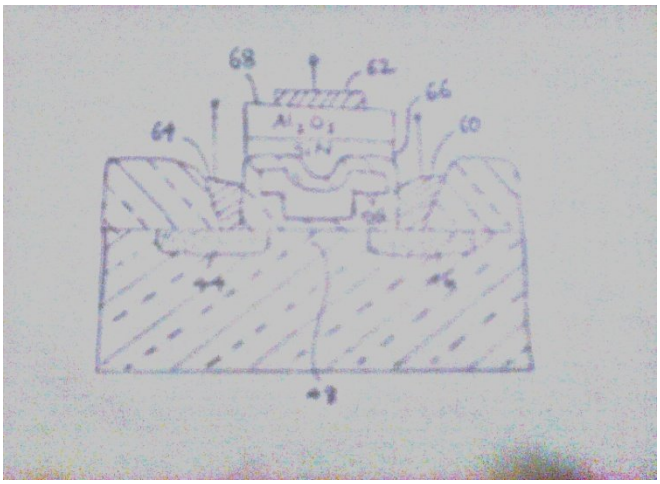


Fig 2.9

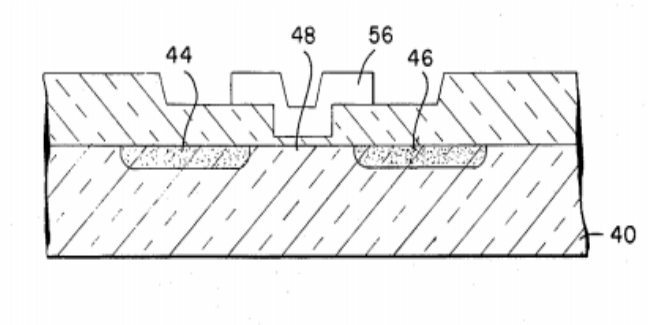


Fig 2.7

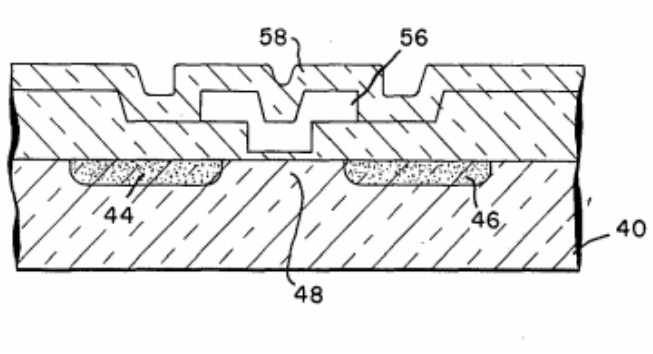


Fig 2.8

As shown in Fig. 2.1 a $SiO_2$ layer 42 is grown over the substrate 40 initially. The source 44, drain 46 & channel 48 are formed and are depicted in Fig. 2.2. Here a portion of $SiO_2$ layer has been removed through convetional masking and etching operations for the formation of active region of transistor [5][12][13].

Silicon dioxide 50 is then grown over the entire surface in wet or dry oxidation ambient from temperature of 900 $^oC$ to 1100 $^oC$. Rapid thermal annealing is done in $N_2$ enviornment for 20 minutes.The high temperature exposure serves to further drive in and activate the dopants into the source 44, channel 48 and drain 46 regions. This can be seen in Fig. 2.3. The next figure shows a processed structure after a predetermined portion 52 of $SiO_2$ 50 was removed through etching [5] [12][13].

Refering to Fig 2.5, a second thermal oxidation step is perfirmed in order to grow a thin $SiO_2$ layer 54. This oxidation is done at low temperature typically from 850 $^oC$ to 950 $^oC$ for about 3 to 10 minutes so that it has a thickercontrol over the oxide thickness. If carried out in dry oxygen ambient, the resulting $SiO_2$ layer 54 in opening 52 will have a thickness typically in the range of 20 to 100 Å. This process can be followed by 10 to 20 minute anneal in nitrogen atmosphere at 800 $^oC$ to 1100 $^oC$ [5] [12][13].

Fig. 2.6 shows the process of formation of floating gate. For this processa layer 56 of the resistive material such as polycrystaline silicon is deposited over the entire surface. After the etching of the polysilicon layer, everywhere else than channel, we get the floating gate seen in Fig. 2.7. Then the polycrystaline layer 56 is oxidized for electrical isolation from the second gate electron which is to be formed in the next step. It is oxidized in dry or wet ambient at temperature from 900 $^oC$ to 1100 $^o$Cand then annealing is done for 20 minutes at 1000 $^oC$ In Fig 2.8 the new layer of $SiO_2$ 58 can be seen [5] [12][13].

Over this oxide layer a 7nm thin SiN 66 is grown by low pressure chemical vapour deposition as shown in Fig. 2.9. Again on this layer, another 15 nm $Al_2O_3$ layer 68 is grown by atomic layer deposition. Thus an Oxide-Nitride-Aluminum

(ONA) stack is created. Annealing is then done in an $N_2$ ambient at 1080 $^oC$ for 2 minutes [2].

The $Al_2O_3$ is fluorinated using a low energy flourine beam of approximately 10eV.The $Al_2O_3$ layer is exposed to the beam for about 15 minutes. The amount of flourine ions that get into the $Al_2O_3$ layer reached a maximum at the surface and decreased rapidly with increasing depth. A loss of O on the $Al_2O_3$ surfacewas observed till a depth of 5nm [2].

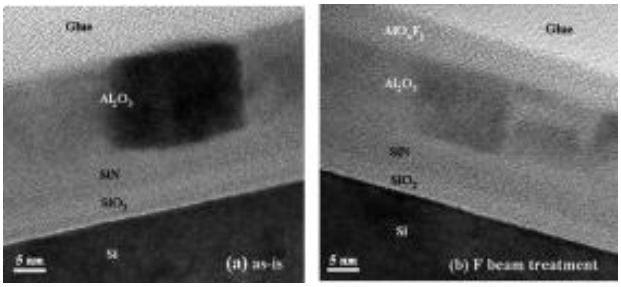


Fig 3

Before the treatment, the $Al_2O_3$ layer was crystallized. Fig 3 shows that untreated ONA stack contains 15nm thick $Al_2O_3$ and 7nm thick SiN. After the stack was exposed to the beam, the total thickness of ONA stack was similar proving that no etching occurred due to the flourine exposure. But, after the beam treatment, the aluminum oxide was divided into 2 layers composed of a top $AlO_xF_y$ layer and bottom $Al_2O_3$ layer.The $AlO_xF_y$ layer was amorphous and approximately 5nm thick, which is the penetration depth of $F^+$ ions in ONA stack [2].

## CONCLUSION

The low energy fluorine beam treatment of ONA stackforms a 5nm thick $AlO_xF_y$ layer over $Al_2O_3$ surface by replacing Al-O bond with Al-F bond. The formation of $AlO_xF_y$ layer showed enhanced charge trapping characteristics. Also the beam treatment ONA stack showed a slightly lower leakage current than the untreated ONA stack. As electron trapping characteristic of floating gate in EEPROM is the important principle behind its operation, the layer of $Al_2O_3$ which has a higher k dielectric than silicon dioxide can prove to be favorable.

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